IN THE CLAIMS

1. (Original) A semiconductor multi-chip package comprising:

a package substrate including a surface having a plurality of bonding tips formed thereon; and

two or more semiconductor chips mounted on the substrate surface, the two or more semiconductor chips each including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region,

wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein each bonding tip is electrically connected to a corresponding one of the bond pads.

2. (Original) The multi-chip package of claim 1, wherein the two or more chips are disposed next to each other.

3. (Original) The multi-chip package of claim 1, wherein the two or more chips are vertically stacked.

4. (Original) The multi-chip package of claim 1, wherein the two or more chips comprise the same type of chips.

5. (Original) The multi-chip package of claim 1, wherein the two or more chips comprise at least a lower chip and an upper chip, the upper chip disposed over the lower chip, and wherein the width of the upper chip is smaller than the width of the lower chip.

6. (Original) The multi-chip package of claim 1, wherein one of the two or more chips is a memory chip and the other chip is a non-memory chip.

7. (Original) The multi-chip package of claim 1, wherein one of the two or more chips is a DRAM and the other chip is a flash memory.

8. (Original) The multi-chip package of claim 1, wherein the bond pads are formed along sides of the semiconductor substrate.

9. (Original) The multi-chip package of claim 1, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

10. (Original) The multi-chip package of claim 1, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

11. (Original) The multi-chip package of claim 1, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

12. (Original) A semiconductor multi-chip package, comprising:

a lead frame having a front surface and a back surface;

a first chip having an upper surface and a lower surface, the upper surface of the first chip disposed under the back surface of the lead frame, the first chip having bond pads formed substantially along a center region of the upper surface; and

a second chip having an upper surface and a lower surface, the upper surface of the second chip disposed under the lower surface of the first chip, the second chip including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region,

wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein the bond pads of the first chip are electrically connected to the lead

frame, and wherein the bond pads of the second chip are electrically connected to the lead frame.

13. (Original) The multi-chip package of claim 12, wherein the bond pads are formed along sides of the semiconductor substrate.

14. (Original) The multi-chip package of claim 12, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

15. (Original) The multi-chip package of claim 12, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

16. (Original) The multi-chip package of claim 12, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

17. (Original) A semiconductor multi-chip package comprising:

a lead frame including a die pad and a lead, the die pad having a front surface and a back surface; and

a first chip disposed over the front surface of the die pad and a second chip disposed over the back surface of the die pad, the first and the second chip each including:

a semiconductor substrate having integrated circuits formed on a cell region and a peripheral circuit region adjacent to each other;

a bond pad-wiring pattern formed on the semiconductor substrate; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, the pad-rearrangement pattern including bond pads disposed over at least a part of the cell region,

wherein the bond pad-wiring pattern is formed substantially in a center region of the semiconductor substrate,

wherein the bond pads of the first and second chips are each electrically connected to the lead.

18. (Original) The multi-chip package of claim 17, further comprising

an additional chip disposed over at least one of the first and second chips, the additional chip having peripheral pads, the peripheral pads are electrically connected to the lead.

19. (Original) The multi-chip package of claim 17, wherein the width of the additional chip is smaller than the width of the first or second chip.

20. (Original) The multi-chip package of claim 17, wherein the bond pads are formed along sides of the semiconductor substrate.

21. (Original) The multi-chip package of claim 17, wherein a portion of the pad-rearrangement pattern extends substantially from the center region of the semiconductor substrate toward an edge of the semiconductor substrate.

22. (Original) The multi-chip package of claim 17, wherein the bond pad-wiring pattern is form on a portion of the peripheral circuit region and extends across a portion of the cell region.

23. (Original) The multi-chip package of claim 17, wherein the bond pad-wiring pattern is formed entirely within the peripheral circuit region.

24. (Previously presented) A multi-chip package comprising:

a first chip; and

a second chip formed over the first chip,

wherein the first chip includes:

a bond pad-wiring pattern formed substantially in a center region of the first chip; and

a pad-rearrangement pattern electrically connected to the bond pad-wiring pattern, wherein the pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip.

25. (Previously presented) The multi-chip package of claim 24, wherein the pad-rearrangement

pattern includes a second bond pad, and wherein the first and second bond pads are respectively disposed along opposing edges of the first chip.

26. (Previously presented) The multi-chip package of claim 25, wherein the pad-rearrangement
pattern extends substantially from the center region of the first chip toward the edge of the first chip.

27. (Previously presented) The multi-chip package of claim 24, wherein the bond pad-wiring
pattern is formed on a first surface of the first chip, and wherein the second chip is mounted on the first surface of the first chip.

28. (Previously presented) The multi-chip package of claim 27, further comprising a spacer
interposed between the first chip and the second chip.

29. (Previously presented) The multi-chip package of claim 24, further comprising a substrate on
which the first chip is mounted.

30. (Previously presented) The multi-chip package of claim 29, wherein the substrate comprises
a printed circuit board, a tape wiring substrate or a lead frame.

31. (Previously presented) The multi-chip package of claim 29, wherein the first and second
chips are mounted respectively on opposite first and second surfaces of the substrate.

32. (Previously presented) The multi-chip package of claim 31, further comprising an additional
chip disposed over at least one of the first and second chips, wherein the width of the additional chip is smaller than the width of the at least one of the first and second chips.

33. (Previously presented) The multi-chip package of claim 24, wherein the first bond pad is
disposed under the second chip.

34. (Previously presented) The multi-chip package of claim 24, wherein the first and second chips
comprise the same type of chips.

35. (Previously presented) The multi-chip package of claim 24, wherein the width of the second
chip is smaller than the width of the first chip.

36. (Previously presented) The multi-chip package comprising:

a first chip; and

a second chip formed over the first chip,

wherein the second chip includes:

a second bond pad-wiring pattern formed substantially in a center region of the second chip; and

a second pad-rearrangement pattern electrically connected to the second bond pad-wiring pattern, wherein the second pad-rearrangement pattern includes a second bond pad disposed at an edge of the second chip.

37. (Previously presented) The multi-chip package of claim 36, wherein the first chip includes:

a first bond pad-wiring pattern formed substantially in a center region of
the first chip; and

a first pad-rearrangement pattern electrically connected to the first

bond pad-wiring pattern, wherein the first pad-rearrangement pattern includes

a first bond pad disposed at an edge of the first chip.

38. (Previously presented) The multi-chip package of claim 37, wherein the first bond pad-wiring

pattern is formed on a first surface of the first chip, and wherein the second chip is mounted on the first surface of the first chip.

39. (Previously presented) The multi-chip package of claim 36, wherein the width of the second

chip is smaller than the width of the first chip.

40. (Previously presented) The multi-chip package of claim 36, further comprising a substrate on

which the first chip is mounted.

41. (Previously presented) The multi-chip package of claim 40, wherein the substrate is a lead frame.

42. (Previously presented) The multi-chip package of claim 40, wherein the first chip includes a

center pad-type bond pad.

43. (Previously presented) The multi-chip package of claim 40, wherein the center pad-type bond

pad is formed on a first surface of the first chip, and wherein the first surface of the first chip is adjacent to the supporting substrate.

44. (Previously presented) The multi-chip package of claim 43, wherein the second chip is

mounted on a second surface of the first chip, the second surface of the first chip being opposite the first surface of the first chip.

44. (Previously presented) A multi-chip package comprising:

first and second chips disposed on an upper surface of a substrate;

wherein the first chip includes:

a first bond pad-wiring pattern formed substantially in a center region of the first chip; and

a first pad-rearrangement pattern electrically connected to the first bond pad-wiring pattern, wherein the first pad-rearrangement pattern includes a first bond pad disposed at an edge of the first chip,

wherein the first and second chips are laterally spaced from each other.

45. (Previously presented) The multi-chip package of claim 44, wherein the second chip includes:

a second bond pad-wiring pattern formed substantially in a center region of the second chip; and

a second pad-rearrangement pattern electrically connected to the second bond pad-wiring pattern, wherein the second pad-rearrangement pattern includes a second bond pad disposed at an edge of the second chip.

46. (Previously presented) A semiconductor multi-chip package comprising:

a first chip mounted on a package substrate; and

an second chip mounted on the first chip with a spacer disposed therebetween, wherein the first chip includes:

bond pad-wiring patterns formed substantially in a center region of the first chip; and

pad-rearrangement patterns electrically connected to the bond pad-wiring patterns, wherein the pad-rearrangement patterns include bond pads disposed along opposing edges of the first chip, wherein the spacer is placed between the bond pads.